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Comparison of FPGA-based Direct Torque Controllers for Permanent Magnet Synchronous Motors

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ABSTRACT

This paper compares two types of direct torque controllers for permanent magnet synchronous motors(PMSMs). These controllers both use a single-chip FPGA(Field Programmable Gate Array) but have differing hardware configurations. One of the controllers was constructed by programming a soft-core CPU and hardware logic circuits written in VHDL(Very high speed IC Hardware Description Language), while the other was constructed of only hardware logic circuits.

The characteristics of these two controllers were compared in this paper. The results show the controller constructed of only hardware logic circuits was able to shorten the control period and it was able to suppress the low torque ripple.

Keywords: Permanent Magnet Synchronous Motor, Field Programmable Gate Array, Direct Torque Control

1. Introduction

Direct torque control (DTC) was proposed by Takahashi for induction machines in the mid-1980s[1]. DTC is an applicable control scheme for all AC motors[2]. In recent years, a significant body of research on DTC has been performed all over the world[3]-[8]. Fig. 1 shows a block diagram of DTC. As shown in this figure, the controller configuration for DTC is simpler than that of conventional current control based vector controls, since the coordinate transformation from a stationary reference frame to a synchronously rotating reference frame or the inverse transformation is not required in DTC. On the other hand, torque- and flux-ripples grow larger when the control period is longer. In order to reduce those ripples, many schemes have been proposed[9]-[13]. Obviously, the ripples can be reduced by shortening the control period. The authors described a PMSM (Permanent Magnet Synchronous Motor) controller using an FPGA (Field Programmable Gate Array) in which the control period of the DTC can be advantageously shortened in an easy control scheme using logic circuits[15]. The controller was constructed by programming hardware logic circuits written in VHDL (Very high speed IC Hardware Description Language) and a soft-core CPU onto a FPGA. This controller is called "*Type A controller*" in this paper.

In recent years, the progress of FPGA-related technologies has been remarkable. Under current conditions, large-scale FPGAs decreases in price year by year, and can be obtained easily. In this paper, a direct torque controller is newly constructed of only hardware

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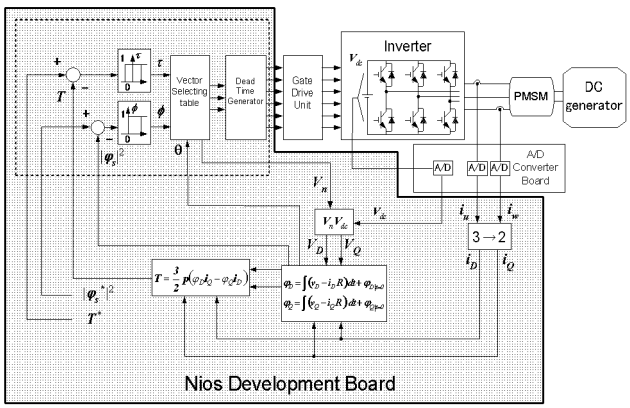


Fig. 1 Block diagram of DTC for PMSM

and called "*Type B controller*". In order to compare the control characteristics of *Type A* and *Type B controllers*, an IPMSM(Interior PMSM) was driven with each controller.

2. Principle of Direct Torque Control

In DTC, torque T, stator flux-linkage amplitude $|\varphi_s|$ and stator flux-linkage position θ_n are estimated from stator currents i_u, i_w and voltage-vector V_n is determined by the conduction state of the inverter switching devices shown in Fig. 1. Torque T and stator flux-linkage amplitude $|\varphi_s|$ are compared with each reference value by hysteresis comparators. The voltage-vector is selected by using these comparator outputs τ, ϕ and the stator flux-linkage position θ_n according to Table 1. Torque T, stator flux-linkage amplitude $|\varphi_s|$ and stator flux-linkage position θ_n is obtained as follows. The instantaneous values of the direct- and quadrature-axis on a stationary reference frame were used in the following calculations; and the values are expressed by subscript D and Q, respectively. In DTC, i_u and i_w are converted into i_D and i_Q by

$$i_D = i_u \tag{1}$$

$$i_Q = -\frac{1}{\sqrt{3}}(i_u + 2i_w)\,. \tag{2}$$

Moreover, V_D and V_Q are calculated by the following equations using the inverter DC-link voltage V_{dc} and coefficients k_D, k_Q. The coefficients are related to the output voltage-vector V_n and are shown in Table 2.

Table 1 Inverter output voltage-vector selecting table for DTC

ϕ	τ	θ_n ($D_2D_1D_0$)					
		θ_1(001)	θ_2(010)	θ_3(011)	θ_4(100)	θ_5(101)	θ_6(110)
ϕ=1	τ=1	V_2(110)	V_3(010)	V_4(011)	V_5(001)	V_6(101)	V_1(100)
	τ=0	V_6(101)	V_1(100)	V_2(110)	V_3(010)	V_4(011)	V_5(001)
ϕ=0	τ=1	V_3(010)	V_4(011)	V_5(001)	V_6(101)	V_1(100)	V_2(110)
	τ=0	V_5(001)	V_6(101)	V_1(100)	V_2(110)	V_3(010)	V_4(011)

Table 2 The coefficients for determining D-Q axis voltage

V_n	k_D	k_Q
V_1	$k_D = 1$	$k_Q = 0$
V_2	$k_D = 1/2$	$k_Q = \sqrt{3}/2$
V_3	$k_D = -1/2$	$k_Q = \sqrt{3}/2$
V_4	$k_D = 1$	$k_Q = 0$
V_5	$k_D = -1/2$	$k_Q = -\sqrt{3}/2$
V_6	$k_D = 1/2$	$k_Q = -\sqrt{3}/2$

$$V_D = \frac{2}{3}k_D V_{dc} \tag{3}$$

$$V_Q = \frac{2}{3}k_Q V_{dc} \tag{4}$$

From i_u, i_w, V_D and V_Q obtained by the above calculations, stator flux-linkage φ_D, φ_Q are estimated by (5) and (6).

$$\varphi_D = \int (V_D - Ri_D)\,dt + \varphi_{D|t=0} \tag{5}$$

$$\varphi_Q = \int (V_Q - Ri_Q)\,dt + \varphi_{Q|t=0} \tag{6}$$

From φ_D, φ_Q, i_u and i_w, the square of the estimated stator flux-linkage $|\varphi_s|^2$ and estimated torque T are calculated by the following equations:

$$|\varphi_s|^2 = {\varphi_D}^2 + {\varphi_Q}^2 \tag{7}$$

$$T = \frac{2}{3}p(\varphi_D i_Q - \varphi_Q i_D)\,, \tag{8}$$

where p is the number of pole-pairs. In addition, stator flux-linkage position θ_n is obtained from φ_D and φ_Q.

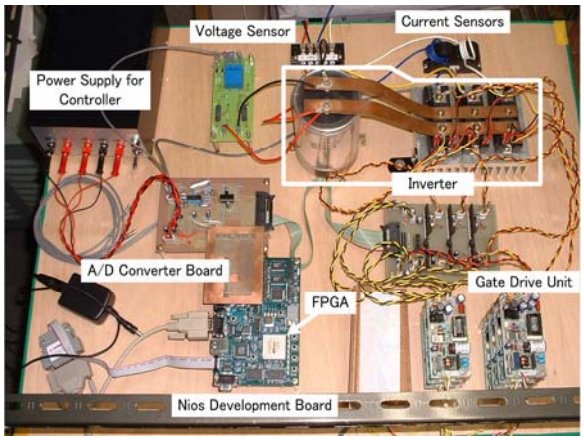


Fig. 2 Photo of the constructed control system

3. Controller Configurations

The control system in this paper was constructed by connecting a gate drive unit and an A/D converter board that acquires the information from current and voltage sensors, to an *Altera Nios Development board, Stratix Edition*[16]. In the A/D converter board, three A/D converters with serial transmission(*National Semiconductor ADC10731*[17]) were used for the acquisition of the measurement data i_u, i_w and V_{dc} from current sensors and a voltage sensor.

The appearance of the constructed control system is shown in Fig. 2. Two types of controllers in this paper shared this system in Fig. 2, because these are realizable only by changing the hardware logic circuits' structure programmed on the FPGA. The performance and the resource utilization of the two controllers(*Type A controller* and *Type B controller*) were compared using this system.

3.1 Type A controller

A functional block diagram of the *Type A controller* is shown in Fig. 3. The *Type A controller* was constructed by programming hardware logic circuits written in VHDL and a soft-core CPU. Two hysteresis comparators, an inverter output voltage-vector selecting table, dead time generators, and subtracters for reference values and estimated values were implemented by hardware logic circuits (the part surrounded by the dotted line in Fig. 1). On the other hand, the following functions are executed on the CPU.

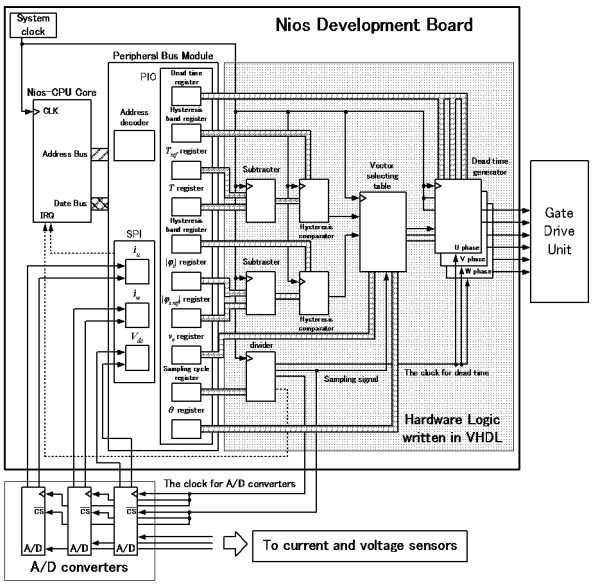


Fig. 3 Functional block diagram of *Type A controller*

- Initializing of the hardware logic circuits written in VHDL (setting bandwidth for the hysteresis comparators, control period and dead time),
- Conversion to parallel data from serial data that are from A/D converters,
- Calculation of torque T, the square of stator flux-linkage amplitude $|\varphi_s|^2$ and stator flux-linkage position θ_n from current values i_u, i_w and inverter output voltage-vector V_n,
- Output of the calculation results to the hardware logic circuits.

In order to shorten the arithmetic processing cost, 16 bits fixed-point arithmetic was carried out in most parts of the above calculations, and 32 bits fixed-point arithmetic was carried out only at integral computation parts which required high accuracy. In addition, estimated flux-linkage $|\varphi_s|$ was compared with reference $|\varphi_s^*|$ at the square value because it reduced the arithmetic processing time. The processing time of the *Type A controller* for the DTC is 50μs.

3.2 Type B controller

In this controller, the following functions which were realized by software in the *Type A controller* were changed to hardware implementation.

- Conversion to parallel data from serial data that were from the A/D converters,

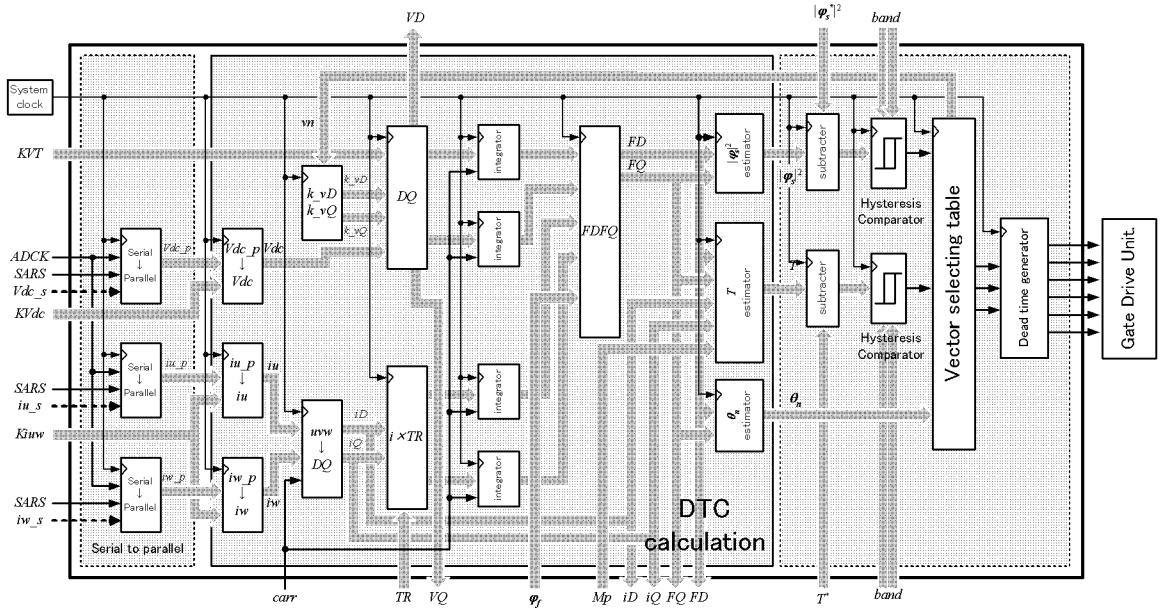


Fig. 4 Functional block diagram of *Type B controller*

- All the calculations for the DTC,

A functional block diagram of the *Type B controller* is shown in Fig. 4. In addition, an explanation of the signals in Fig. 4 is shown in Table 3. As in the *Type A controller*, 32 bits fixed-point arithmetic was carried out only at integral computation parts; and 16 bits fixed-point arithmetic was carried out in the rest of the calculations. Also, a parallel operation was carried out to reduce the arithmetic processing time as shown in Fig. 4.

The CPU performed the following functions:

- initializing of the hardware logic circuits described in VHDL,
- data acquisition of the operation results (V_D, V_Q, i_D, i_Q, φ_D, φ_Q, $|\varphi_s|^2$, T, θ_n) for verification in the experiments.

The time-line diagram of the *Type B controller* is shown in Fig. 5. The processing time of the *Type B controller* is 20.34μs as shown in Fig. 5. However, most of this time is occupied by acquisition, analog-to-digital conversion and serial-to-parallel conversion. These depend on the performance of the A/D converters; the calculation of the DTC hardly requires time. Therefore, when the A/D converters used in this paper are changed to high-speed A/D converters, a shorter control period is expected.

Table 3 Explanation of the signals in Fig. 4

ADCK	Clock for A/D converters.
SARS	Successive approximation register status of A/D converter.
Vdc_s	Serial data of A/D conversion result of dc link voltage.
iu_s, iw_s	Serial data of A/D conversion result of *u*- and *w*-phase stator current.
KVT	$2/3 \times T_s$ (T_s: Sampling period.)
vn	Voltage vector selected by inverter output voltage-vector selecting table.
KVdc, Kiuw	Conversion coefficients for A/D converter.
carr	Synchronization signal for latch circuits.
TR	$T_s \times R$ (R: Stator resistance.)
φ_f	Magnet flux-linkage.
Mp	$3/2 \times p$ (p: Number of pole-pairs.)
VD,VQ	Voltages on the D-Q coordinate.
iD, iQ	Stator currents on the D-Q coordinate.
FD, FQ	Flux-linkages on the D-Q coordinate.
$\lvert\varphi_s\rvert^2$	Square of estimated stator flux-linkage.
T	Estimated torque.
θ_n	Estimated stator flux-linkage position.
$\lvert\varphi_s^*\rvert^2$	Square of reference stator flux-linkage.
T^*	Reference torque.
band	Hysteresis band.

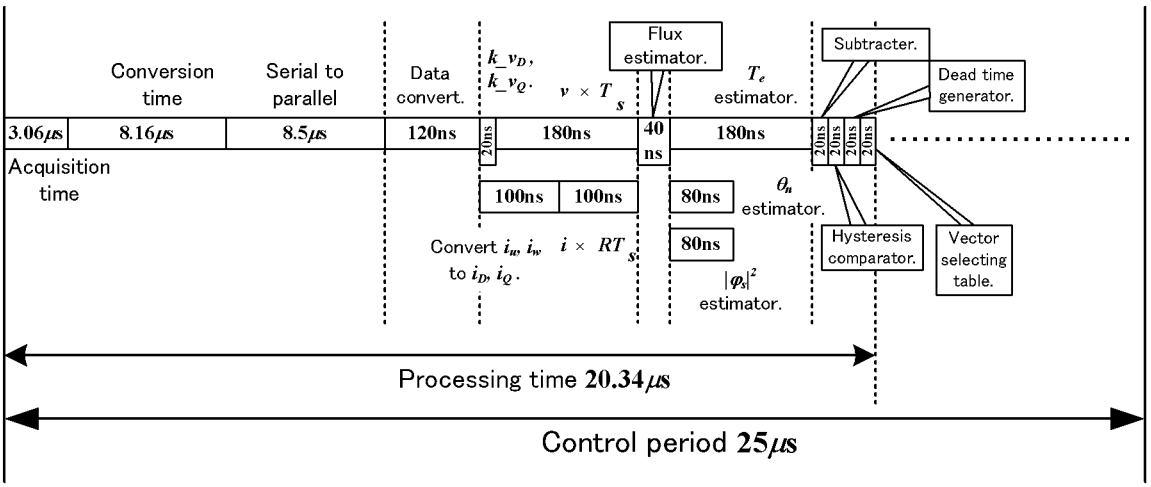


Fig. 5 Time-line diagram of *Type B controller*

4. Characteristics comparison of two controllers

Tables 4 and 5 are the FPGA resource utilization for the *Type A* and *Type B controllers*, respectively. By changing the controller configuration, the rate of total logic elements increased from 35% to 53%.

In order to compare the control characteristics of *Type A* and *Type B controllers*, IPMSM was driven with each controller. The motor parameters of the IPMSM used for the experiments are shown in Table 6. Torque reference T^*, flux-linkage reference $|\varphi_s^*|$ and inverter DC-link voltage V_{dc} were set up as 8N-m, 0.289035Wb and 100V, respectively. Besides, the base clock of both systems is 50MHz.

Table 4 FPGA resource utilization of *Type A controller*

Total logic elements	**3,737 / 10,570 (35%)**
Total pins	123 / 426 (28%)
Total memory bits	34,688 / 920,448 (3%)
DSP block 9-bit elements	**2 / 48 (4%)**
total PLLs	0 / 6 (0%)
Total DLLs	0 / 2 (0%)

Table 5 FPGA resource utilization of *Type B controller*

Total logic elements	**5,622 / 10,570 (53%)**
Total pins	123 / 426 (28%)
Total memory bits	34,688 / 920,448 (3%)
DSP block 9-bit elements	**30 / 48 (62%)**
total PLLs	0 / 6 (0%)
Total DLLs	0 / 2 (0%)

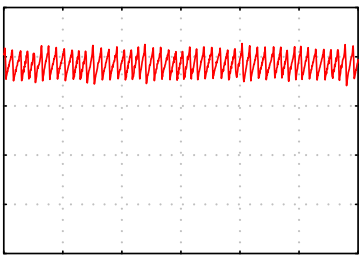
Figs. 6 and 7 show the experimental results for the *Type A* and *Type B controllers*, respectively. The minimum control period of the *Type A controller* is 50μs. On the other hand, the period of the *Type B controller* could be 25μs (Processing time was 20.34μs; however the control period was set as 25μs because of the limitations of the gate drive unit.). As a result, the torque ripple width of the *Type A controller* is 1.2N-m, and that of the *Type B controller* is 0.8N-m.

Table 6 Motor parameters

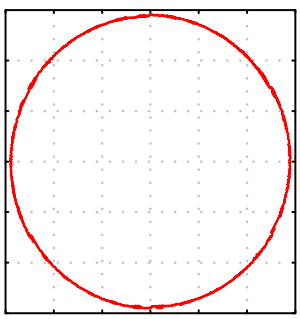
Rated speed	N_R	1800 [rpm]
Number of pole-pairs	p	2
Stator resistance	R	0.5919 [Ω]
d axis inductance	L_d	10.54 [mH]
q axis inductance	L_q	26.56 [mH]
Magnet flux-linkage	φ_f	0.19129 [Wb]

5. Conclusions

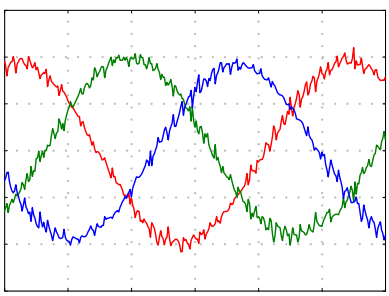
If all control functions are constructed from only hardware, processing time can be decreased; on the other hand, the number of logic elements increases. By changing the controller configuration from the *Type A controller* to the *Type B controller*, processing time is decreased from 50μs to 20.34μs. On the other hand, the rate of total logic elements increased from 35% to 53%. Since large-scale FPGAs can be obtained at low-cost in recent years; it is therefore possible to construct a



(a) Torque

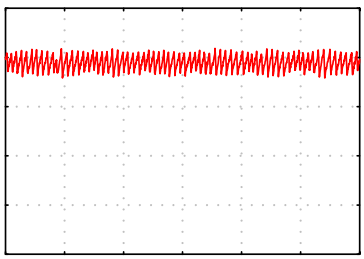


(b) Flux

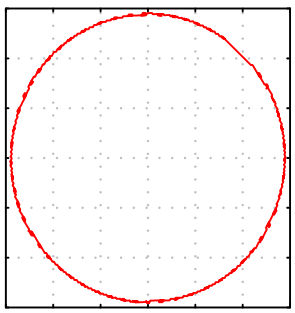


(c) Current

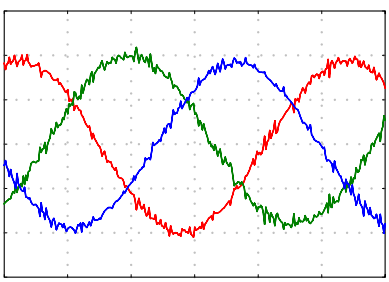
Fig. 6 Experimental results using *Type A controller* at T_s=50μs.



(a) Torque



(b) Flux



(c) Current

Fig. 7 Experimental results using *Type B controller* at T_s=25μs.

controller by using only hardware. A hardware configured controller using an FPGA is effective in the reduction of torque- and flux-ripples.

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